AMENDMENTS TO THE CLAIMS

1. (Original) A method of performing a measurement on a differential signal, comprising:

a) providing each leg of the differential signal to an input of a comparator having at least a first and second input;

b) introducing a plurality of bias levels into the comparison, whereby the output of the comparator is a first logical value when the value at the first input exceeds the value at the second input by the bias level;

c) taking a plurality of sets of samples of the output of the comparator, with a set of samples for each of the bias levels, each of the samples in each of the sets correlated in time to a point on the waveform;

d) selecting a set of samples having values with a predetermined percentage of a predetermined logical value; and

e) associating the bias value used to take the samples in the selected set with the value of the differential signal at the point on the waveform.

2. (Original) The method of claim 1 wherein introducing a bias level comprises passing a current through a resistor connected to one of the first and second inputs of the comparator.

3. (Currently amended) The method of claim [[2]] 1 wherein introducing a plurality of bias ~~level~~ levels comprises passing a first current through a first resistor connected to the first input of the comparator and passing a second current through a second resistor connected to the second input of the comparator, with the plurality of bias levels introduced by altering the relative level of the first current and the second current.

4. (Original) The method of claim 2 wherein the comparator is contained inside a commercially available component having leads accessible at its exterior, including exterior leads coupled to the first and second inputs of the comparator.

5. (Original) The method of claim 4 wherein the resistor is outside the commercially available component and coupled to an input of the comparator.

6. (Original) The method of claim 2 wherein each leg of the differential signal is AC coupled to one of the first and second inputs to the comparator.

7. (Original) The method of claim 1 wherein introducing a bias level comprises altering the operating characteristics of the comparator.

8. (Original) The method of claim 1 wherein the comparator is contained inside a commercially available component having leads accessible at its exterior, including exterior leads coupled to the first and second inputs of the comparator and introducing a bias level comprises applying an electrical signal to at least one of the leads coupled to the first and second inputs of the comparator.

9. (Currently amended) The method of claim 1 wherein the differential signal has a plurality of rising edges and taking samples correlated in time to a point ~~in~~on the waveform comprises setting strobe times at which the comparator takes samples to be at a predetermined time relative to the start of a rising edge.

10. (Original) A method of manufacturing a semiconductor component incorporating the method of claim 1 wherein the differential signal is an output of the semiconductor component at a stage in its manufacture and steps b) through e) of claim 1 are repeated to associate values with a plurality of points on the differential signal.

11. (Currently amended) The method of claim 10 wherein the method of manufacturing the semiconductor component comprises:

performing an analysis of the semiconductor component using the values associated with the plurality of points on the differential signals; ~~are used to analyze the performance of the semiconductor component~~ and

selecting at least one step in the manufacturing process ~~subsequent steps in the manufacturing process of the semiconductor component are selected~~ in response to the analysis.

12. (Original) A process of making semiconductor devices using the method of claim 1, the process comprising:

a) connecting a semiconductor device under test to a test system;

b) stimulating the device under test with signals from the test system;

c) providing a differential signal generated by the device under test to the test system and performing, with the test system, the steps of claim 1 to provide parameters of the differential signal;

d) using the parameters of the differential signal to adjust the manufacturing process for making semiconductor devices.

13. (Original) The process of making semiconductor devices of claim 12 wherein adjusting the manufacturing process comprises speed binning the device under test.

14. (Original) An automatic test system suitable for making measurements of a differential signal applied as an input to the test system, the test system having a measurement circuit comprising:

a) a comparator having:

i) a first and second signal input terminals

ii) an output providing a logical signal indicating the results of a comparison; and

iii) a timing input controlling the time at which a comparison is made;

b) means for biasing the comparison by a variable amount in response to a control signal;

c) control circuitry providing a timing signal connected to the timing input of the comparator and a control signal to the means for biasing; and

d) data analysis circuitry having an input coupled to the output of the comparator, the data analysis circuitry determining parameters of the differential signal from the output of the comparator.

15. (Original) The automatic test system of claim 14 wherein the input terminals of the comparator are AC coupled to the input of the test system and the means for biasing the comparison comprises at least one voltage source coupled to at least one of the first and second input terminals of the comparator.

16. (Original) The automatic test system of claim 15 wherein the voltage source comprises a current source and a resistor with the resistor connected to the current source and an input terminal of the comparator.

17. (Original) The automatic test system of claim 15 wherein the comparator is enclosed in semiconductor packaging with the first and second input terminals accessible through leads on the outside of the package.

18. (Currently amended) The automatic test system of claim 17 wherein the comparator is part of a commercially available semiconductor ~~component,~~ component.

19. (Original) The automatic test system of claim 18 wherein the commercially available semiconductor component comprises a differential receiver.

20. (Original) The automatic test system of claim 19 wherein the commercially available semiconductor component comprises a Gigabit receiver.

21. (Original) The automatic test system of claim 14 wherein the comparator is a portion of an instrument installed in the automatic test system.

22. (Original) The automatic test system of claim 14 wherein the test system includes the timing generator and the control circuitry comprises the timing generator.

23. (Original) The automatic test system of claim 14 wherein the data analysis circuit comprises a general purpose computer programmed to determine parameters of the differential signal.

24. (Original) The automatic test system of claim 23 wherein the data analysis circuit comprises a user interface through which the eye pattern of the differential signal is displayed.